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October 31, 2005

U.S. Patent & Trademark Office
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To Whom It May Concern:

Enclosed please find documents listed below that were mailed to our firm; these documents do not appear to belong to us:

10/765,175	Notice of Allowability
11/090,541	Notice Regarding Change of Power of Attorney

Thank you,

Justin Lancaster
U.S. Docketing Clerk
(949)721-5273

Notice of Allowability

Application No.	Applicant(s)	
10/765,175	TOYODA ET AL.	
Examiner	**Art Unit**	
MATTHEW V. NGUYEN	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed 1/28/04*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/30/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Matthew V. Nguyen
MATTHEW V. NGUYEN
PRIMARY EXAMINER

The International Search Report and the Information Disclosure Statement filed on 6/30/04 along with all the references cited therein have been considered.

2. The following is an examiner's statement of reasons for allowance: none of prior art of record taken alone or in combination shows a voltage generating circuit and a method thereof comprising a first capacitor, a second capacitor, a third capacitor, an output terminal, a supply voltage terminal, a first switch, a second switch along with specific electronic connections among those elements and particular functions thereof, and more detailed elements as recited in the claims of the instant application.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew V. Nguyen whose telephone number is (571) 272-2081.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-2800.

Matthew V. Nguyen

MATTHEW V. NGUYEN
PRIMARY EXAMINER

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Alexandria, Virginia 22313-1450

or Fax **(571) 273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 09/27/2005

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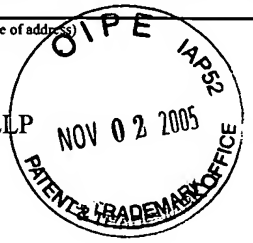

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Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,175	01/28/2004	Kenji Toyoda	63979-039	9845

TITLE OF INVENTION: VOLTAGE GENERATING CIRCUIT, VOLTAGE GENERATING DEVICE AND SEMICONDUCTOR DEVICE USING THE SAME, AND DRIVING METHOD THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	12/27/2005

EXAMINER	ART UNIT	CLASS-SUBCLASS
NGUYEN, MATTHEW VAN	2838	327-536000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____ 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are enclosed:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

☐ A check in the amount of the fee(s) is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

The Director of the USPTO is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.
NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,175	01/28/2004	Kenji Toyoda	63979-039	9845

20995 7590 09/27/2005

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EXAMINER	
NGUYEN, MATTHEW VAN	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/27/2005

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 183 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 183 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571) 272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 09/27/2005

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER
NGUYEN, MATTHEW VAN

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 09/27/2005

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,175	01/28/2004	Kenji Toyoda	63979-039	9845

TITLE OF INVENTION: VOLTAGE GENERATING CIRCUIT, VOLTAGE GENERATING DEVICE AND SEMICONDUCTOR DEVICE USING THE SAME, AND DRIVING METHOD THEREOF

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1400	$300	$1700	12/27/2005

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

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B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 07/05) Approved for use through 04/30/2007.

INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
63979-039	10/765,175
APPLICANT: Kenji TOYODA, et al.	
FILING DATE: January 28, 2004	GROUP: 2838

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code2 (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
MN		US	US 2002/0043676 A1	4/18/2002	Ohtsuka et al	
		US				
		US				
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code3-Number 4-Kind Code5 (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
MN		JP 2003-273352 A	9/26/2003	MATSUSHITA ELECTRIC IND CO LTD		w/English Abstract	
MN		JP 2003-92533 A	3/28/2003	MATSUSHITA ELECTRIC IND CO LTD		w/English Abstract	
MN		JP 5-041080	2/19/1993	OLYMPUS OPTICAL CO LTD		w/English Abstract	
MN		JP 06-119773	4/28/1994	HITACHI LTD		w/English Abstract	
MN		JP 02-188161	7/24/1990	SEIKO EPSON CORP		w/English Abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED
Matthew V. Nguyen	9/24/05

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

Notice of References Cited

Application/Control No.	Applicant(s)/Patent Under Reexamination	
10/765,175	TOYODA ET AL.	
Examiner	Art Unit	Page 1 of 1
MATTHEW V. NGUYEN	2838	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,801,577	09-1998	Tailliet, Fran.cedilla.ois	327/536
	B	US-6,278,315	08-2001	Kim, Yong-Hwan	327/536
	C	US-2003/0201820	10-2003	Katsuhisa, Takuji	327/536
	D	US-2004/0232974	11-2004	Tobita, Youichi	327/536
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
X	N	EP 0576008	06-1993	European Patent	Tsukada	G11C 5/14
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 576 008 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **93110116.6**

(51) Int. Cl.5: **G11C 5/14**, G05F 3/20

(22) Date of filing: **24.06.93**

(30) Priority: **24.06.92 JP 165209/92**

(43) Date of publication of application:
29.12.93 Bulletin 93/52

(84) Designated Contracting States:
DE FR GB

(71) Applicant: **NEC CORPORATION**
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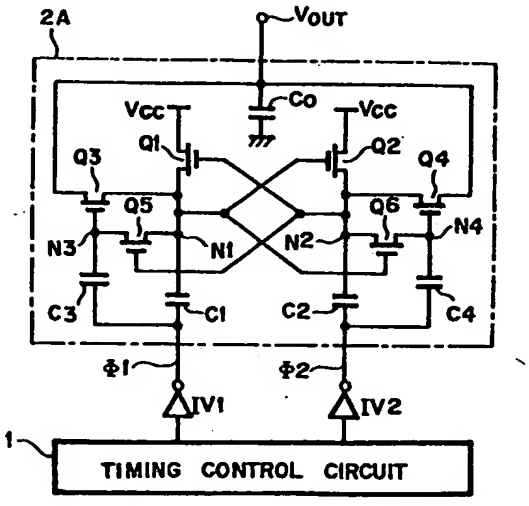
(54) Boost voltage generating circuit.

(57) A boost voltage generating circuit includes a boost voltage producing circuit (2) having a first and a second capacitor receiving a first and a second control signal, respectively, a third smoothing capacitor (C1,C2,C_O) connected at an output terminal (V_{OUT}), and a first, a second, a third, and a fourth transistor (Q1,Q2,Q3,Q4). A boost output voltage is derived through the third and fourth transistors. The boost voltage producing circuit (2) further includes a fourth capacitor (C3) connected between the first capacitor (C1) and the gate of the third transistor (Q3); a fifth capacitor (C4) connected between the second capacitor (C2) and the gate of the fourth transistor (Q4); a fifth transistor (Q5) having one of a source and a drain connected to the first capacitor (C1) with the other thereof connected to the gate of the third transistor (Q3) and a gate connected to the second capacitor (C2); and a sixth transistor (Q6) having one of a source and a drain connected to the second capacitor (C2) with the other thereof connected to the gate of the fourth transistor (Q4) and a gate connected to the first capacitor (C1). The arrangement enables to maintain the gate potential of the third and fourth transistors (Q3,Q4) above a predetermined level, thereby preventing the lowering of current driving capability of these transistors and the lowering of current supplying capability for a boost potential.

FIG. 2A



EP 0 576 008 A2

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to a boost voltage generating circuit, and more particularly to a boost voltage generating circuit for producing a boost potential for a word line of a semiconductor memory device or of a substrate potential for a semiconductor integrated circuit.

(2) Description of the Related Art

An example of the conventional boost voltage generating circuit of the kind to which the present invention relates is shown in Fig. 1A and the waveforms obtained at various points therein are shown in Fig. 1B.

The conventional boost voltage generating circuit referred to above is constituted by a timing control circuit 1 and a boost voltage producing section 2. The timing control circuit 1 outputs a first control signal Φ1 and a second control signal Φ2 respectively through an output node of an inverter IV1 and an output node of an inverter IV2. The first control signal Φ1 becomes a power supply potential (V_{CC}) level and a reference potential (ground potential) level in a predetermined cycle, and the second control signal Φ2 becomes a power supply potential level for a predetermined period within the period of the reference potential level of the first control signal Φ1 and becomes a reference potential level outside the period of the power supply potential level. The boost voltage producing section 2 includes first and second capacitor elements C1 and C2 which receive respectively the first and second control signals Φ1 and Φ2 at their first ends; a first N-channel field effect transistor Q1 in which one of a source and a drain is connected to the power supply potential terminal (V_{CC}), the other of the source and the drain is connected to a second end of the first capacitor element C1, and a gate is connected to the second end of the second capacitor element C2; a second N-channel transistor Q2 in which one of a source and a drain is connected to the power supply potential terminal V_{CC}, the other of the source and the drain is connected to the second end of the second capacitor element C2, and a gate is connected to the second end of the first capacitor element C1; a third N-channel transistor Q3 in which one of a source and a drain, and a gate are connected to the second end of the first capacitor element C1, and the other of the source and the drain is connected to a boost potential output terminal V_{OUT} - (V_{OUT} also representing the boost potential); a fourth N-channel transistor Q4 in which one of a source and a drain, and a gate are connected to the second end of the second capacitor element C2, and the other of the source and the drain is connected to the boost potential output terminal V_{OUT}; and a third capacitor element C_O having a large capacitance which is connected between the boost potential output terminal V_{OUT} and the reference potential terminal.

The operation of the above explained boost voltage generating circuit is as follows.

When the control signal Φ1 is at the power supply potential level V_{CC} and the control signal Φ2 is at the ground potential level (0 V), the transistor Q2 turns ON so that the node N2 at the second end of the second capacitor element C2 is charged and becomes the power supply potential V_{CC}. Also, if the node N1 at the second end of the first capacitor element C1 is at a level higher than V_{OUT} + V_T (V_T being the threshold voltage of the transistor), the current flows from the node N1 to the boost potential output terminal V_{OUT} through the transistor Q3 and thus the boost potential V_{OUT} is raised to a level higher than the power supply potential V_{CC}.

Next, contrary to the above, when the control signal Φ1 turns to the ground potential level and the control signal Φ2 turns to the power supply potential level, the potential at the node N2 rises close to $2V_{CC}$ whereby the transistor Q1 becomes ON and the node N1 is charged up to the level of the power supply potential V_{CC}. Also, the charges are supplied to the boost potential output terminal V_{OUT} through the transistor Q4.

The above operation is repeated and, after being smoothed by the capacitor element C_O having a large capacitance, the boost voltage V_{OUT} is raised to a potential higher than the power supply potential V_{CC}.

The boost voltage V_{OUT} thus obtained is used for such purposes as for select-level driving of word lines of a semiconductor memory device. Also, when the P-channel transistors are employed and the potentials at various points are reversed, it is possible to obtain the substrate potential to be applied to the substrate of a semiconductor integrated circuit.

In the boost voltage generating circuit described above, since the charges of the capacitor element C1 are supplied to the boost potential output terminal V_{OUT} through the transistor Q3 when the control signal Φ1 is at the power supply potential level V_{CC}, the level at the node N1 gradually lowers starting from about $2V_{CC}$ as shown in Fig. 1B. Therefore, the ON-resistance of the transistor Q3 whose gate is directly connected to the node N1 becomes greater, resulting in the lowering of the current driving capability so that, although it is possible to boost the boost potential V_{OUT} almost to $2V_{CC}$ minus V_T, the current supply capability

largely drops once the boost potential V_{OUT} is set to a high level.

SUMMARY OF THE INVENTION

It is, therefore, an object of the invention to overcome the problems existing in the prior art and to provide an improved boost voltage generating circuit in which the current supply capability for boost voltage potentials is enhanced.

According to one aspect of the invention, there is provided a boost voltage generating circuit having a timing control circuit and a boost voltage producing circuit, the timing control circuit being for generating a first control signal to become a power supply potential level and a reference potential level at a predetermined cycle and a second control signal to become the power supply potential level during a predetermined period within a period of the reference potential level of the first control signal and become the reference potential level during a period outside the period of the reference potential level, the boost voltage producing circuit including a first and a second capacitor element receiving respectively at their first ends the first and second control signals, a first transistor having either a source or a drain connected to a power supply potential node with the other of the source and the drain connected to a second end of the first capacitor element and a gate connected to a second end of the second capacitor element, a second transistor having either a source or a drain connected to the power supply potential node with the other of the source and the drain connected to the second end of the second capacitor element and a gate connected to the second end of the first capacitor element, a third transistor having either a source or a drain connected to the second end of the first capacitor element with the other of the source and the drain connected to a boost potential output terminal, a fourth transistor having either a source or a drain connected to the second end of the capacitor element with the other of the source and the drain connected to the boost potential output terminal, and a third capacitor element connected between the boost potential output terminal and a reference potential node, the boost voltage producing circuit further comprising:

a fourth capacitor element connected between the first end of the first capacitor element and the gate of the third transistor;

a fifth capacitor element connected between the first end of the second capacitor element and the gate of the fourth transistor;

a fifth transistor having either a source or a drain connected to the second end of the first capacitor element with the other of the source and the drain connected to the gate of the third transistor and a gate connected to the second end of the second capacitor element; and

a sixth transistor having either a source or a drain connected to the second end of the second capacitor element with the other of the source and the drain connected to the gate of the fourth transistor and a gate connected to the second end of the first capacitor element.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be apparent from the following description of preferred embodiments of the invention explained with reference to the accompanying drawings, in which:

Fig. 1A is a circuit diagram showing a conventional boost voltage generating circuit and Fig. 1B is a chart showing operating waveforms at various points therein;

Fig. 2A is a circuit diagram showing a boost voltage generating circuit of a first embodiment according to the invention and Fig. 2B is a chart showing operating waveforms at various points therein;

Fig. 3A is a circuit diagram showing a boost voltage generating circuit of a second embodiment according to the invention and Fig. 3B is a chart showing operating waveforms at various points therein; and

Fig. 4A is a circuit diagram showing a boost voltage generating circuit of a third embodiment according to the invention and Fig. 4B is a chart showing operating waveforms at various points therein.

PREFERRED EMBODIMENTS OF THE INVENTION

Now, explanation is made of preferred embodiments of the invention with reference to the accompanying drawings. It should be noted that, throughout the explanation, similar reference symbols or numerals refer to the same or similar elements in all the figures of the drawings.

Fig. 2A shows in circuit diagram a first embodiment of the invention and Fig. 2B shows operating waveforms at various points in the circuit of the first embodiment.

The differences in the boost voltage generating circuit of this embodiment as compared with the conventional circuit shown in Figs. 1A and 1B reside in the provision of a fourth capacitor element C3, a fifth capacitor element C4, a fifth field effect transistor Q5, and a sixth field effect transistor Q6. The fourth capacitor element C3 is connected between the first end of the first capacitor element C1 and the gate of the third transistor Q3. The fifth

capacitor element C4 is connected between the first end of the second capacitor element C2 and the gate of the fourth transistor Q4. As to the fifth transistor Q5, one of a source and a drain is connected to the second end of the first capacitor element C1, the other of the source and the drain is connected to the gate of the third transistor Q3, and a gate is connected to the second end of the second capacitor element C2. As to the sixth transistor Q6, one of a source and a drain is connected to the second end of the second capacitor element C2, the other is connected to the gate of the fourth transistor Q4, and a gate is connected to the second end of the first capacitor element C1.

Next, the operation of the circuit according to this embodiment is explained.

When the control signal Φ1 turns to the power supply potential level V_{CC} and the control signal Φ2 turns to the ground potential level, the node N1 and the node N3 rise almost to $2V_{CC}$ so that the transistor Q3 turns ON and thus the current flows from the node N1 to the boost potential output terminal V_{OUT}. Thus, although the potential at the node N1 gradually drops, the node N3 continues to maintain a high potential because the transistor Q5 is in an ON state. Also, the transistor Q6 is in an ON state, so that the gate of the transistor Q4, that is, the node N4 are precharged to the potential at the node N2 with a consequence that the transistor Q4 is turned OFF. Next, when the control signal Φ1 turns to the ground potential level and the control signal Φ2 turns to the power supply potential level, the transistor Q1 is caused to turn ON and the node N1 is charged up to the power supply potential V_{CC},the transistor Q5 turns ON, the node N3 is precharged to a potential which equals that at the node N1, and the transistor Q3 turns OFF. Further, since the potentials at the node N2 and the node N4 have risen to approximately $2V_{CC}$ and the transistor Q4 turns ON, the current is supplied to the power supply potential terminal V_{CC} from the node N2 so that, although the potential of the node N2 gradually drops, it should be noted that the node N4 is maintained at the high potential.

As explained above, even when the potential drops due to the current flow from the nodes N1 and N2 to the boost potential output terminal V_{OUT}, the gate potentials of the transistor Q3 and the transistor Q4 are maintained at high potentials, whereby the possibility of lowering the current driving capability is minimized and the current supplying capability is significantly increased.

Fig. 3A is a circuit diagram showing a boost voltage generating circuit according to the second embodiment of the invention and Fig. 3B is a diagram showing operating waveforms at various points in the circuit. In the above explained first embodiment, at the timings t1 and t2 in Fig. 2B, there is a possibility that the currents may momentarily flow in a reverse direction from the boost potential output terminal V_{OUT} to the nodes N1 and N2 respectively through the transistors Q3 and Q4. This results in wasting power dissipation. The second embodiment of the invention is intended to solve this problem.

According to this second embodiment, the timing control circuit 1A generates through inverters IV3 and IV4 a third control signal Φ3 and a fourth control signal Φ4 in addition to the first and second control signals Φ1 and Φ2. This second embodiment is different from the first embodiment in that the first ends of the fourth and fifth capacitor elements C3 and C4 receive the third and fourth control signals Φ3 and Φ4, respectively, in place of the first and second control signals Φ1 and Φ2. The control signal Φ3 turns to a power supply potential level after the level of the first control signal Φ1 becomes the power supply potential level, and turns to a ground potential level before the level of the first control signal Φ1 becomes the ground potential level. The control signal Φ4 turns to the power supply potential level after the level of the second control signal Φ2 becomes the power supply potential level and turns to the ground potential level before the level of the second control signal Φ2 becomes the ground potential level. The above third control signal Φ3 is supplied to the first end of the fourth capacitor element C3, which end is separated from the first end of the first capacitor element C1 in the first embodiment shown in Fig. 2A. In the same manner, the fourth control signal Φ4 is supplied to the first end of the fifth capacitor element C4, which end is separated from the first end of the second capacitor element C2 in the first embodiment shown in Fig. 2A.

Consequently, when the transistor Q3 turns ON, the level at the node N1 definitely becomes the power supply potential level and, when the transistor Q4 turns ON, the level of the node N4 definitely becomes the power supply potential level. Thus, it is possible to prevent the reverse flow of the current from the boost potential output terminal V_{OUT} to the nodes N1 and N2, so that there is no waste of power unlike in the first embodiment shown in Fig. 2A.

Fig. 4A diagrammatically shows a boost voltage generating circuit of a third embodiment according to the invention, and Fig. 4B shows operating waveforms at various points in such circuit.

In the circuits of the first and second embodiments, the gate level of each of the transistors Q3 and Q4 when it turns ON is in the order of $2V_{CC}$. Strictly speaking, the gate level is lower than $2V_{CC}$ by the potential which is determined by the ratio between the capacitance of each of the capacitor elements C3, C4 and the gate capacitance of each

of the transistors Q3, Q4. As the capacitance of the capacitor elements C3 and C4 increases from the gate capacitance of each of the transistors Q3 and Q4, the gate potential or level will become closer to $2V_{CC}$. However, the boost voltage V_{OUT} will be, even at its maximum, a voltage lower by the threshold voltage V_T of the transistor than a voltage at the state when the gate potential of the transistors Q3 and Q4 is at the power supply potential. This means that the gate level can be raised only close to $(2V_{CC} - V_T)$. The circuit of the third embodiment has improved this point, whereby the gate potential can be raised at the maximum up to almost $2V_{CC}$.

The circuit of the third embodiment is provided with level conversion circuits 3a and 3b in addition to the circuit configuration of the second embodiment shown in Fig. 3A. These level conversion circuits 3a and 3b generate respectively a level-converted third control signal Φ3a and a level-converted fourth control signal Φ4a of high levels in which the power supply potential levels of the third control signal Φ3 and the fourth control signal Φ4 are made higher respectively by predetermined levels. Each of these high level third and fourth control signals Φ3a and 3b is inputted to the corresponding first end of the fourth and fifth capacitor elements C3 and C4.

The control signals Φ3a and Φ4a are produced by buffering the outputs from the timing control circuit 1A at the level conversion circuits 3a and 3b. At this time, the boost voltage potential V_{OUT} is inputted to the level conversion circuits 3a and 3b as an output power supply, whereby the levels of the control signals Φ3a and Φ4a become boosted voltage levels and thus the high levels at the nodes N3 and N4 rise almost to $(V_{CC} + V_{OUT})$. Since the gate levels of the transistors Q3 and Q4 can be raised to the levels higher than those in the circuits of the first and second embodiments, the current driving capability of the transistors Q3 and Q4 becomes large allowing the boost voltage potential V_{OUT} to rise close to $2V_{CC}$ at the maximum.

As explained above, according to the invention, the gate potential levels of the third and fourth transistors are maintained above the predetermined levels by the provision of the fifth and sixth transistors and the fourth and fifth capacitor elements. This enables to prevent the lowering of the current driving capability of the third and fourth transistors and also to prevent the lowering of the current supplying capability for the boost potential, which results in the following advantages:

(1) Where the current supply required is the same as that in the prior art, the size of each of the transistors and the capacitor elements can be made smaller so that, in designing a circuit, the area to be occupied by the circuit can be reduced.

(2) By making the size of each transistor smaller, the current for driving the circuit can be reduced and the current conversion efficiency [= (current supplied to V_{OUT})/(current dissipation from V_{CC})] can be enhanced.

While the invention has been described in its preferred embodiments, it is to be understood that the words which have been used are words of description rather than limitation and that changes within the purview of the appended claims may be made without departing from the true scope and spirit of the invention in its broader aspects.

Claims

1. A boost voltage generating circuit having a timing control circuit (1;1A) and a boost voltage producing circuit (2A;2B;2C), said timing control circuit (1) being for generating a first control signal (Φ1) to become a power supply potential level (V_{CC}) and a reference potential level at a predetermined cycle and a second control signal (Φ2) to become said power supply potential level during a predetermined period within a period of said reference potential level of said first control signal and become said reference potential level during a period outside said period of said reference potential level, said boost voltage producing circuit (2A;2B;2C) including a first and a second capacitor element (C1,C2) receiving respectively at their first ends said first and second control signals (Φ1,Φ2), a first transistor (Q1) having either a source or a drain connected to a power supply potential node with the other of said source and said drain connected to a second end of said first capacitor element (C1) and a gate connected to a second end of said second capacitor element (C2), a second transistor (Q2) having either a source or a drain connected to said power supply potential node with the other of said source and said drain connected to the second end of said second capacitor element (C2) and a gate connected to the second end of said first capacitor element (C1), a third transistor (Q3) having either a source or a drain connected to the second end of said first capacitor element (C1) with the other of said source and said drain connected to a boost potential output terminal (V_{OUT}), a fourth transistor (Q4) having either a source or a drain connected to the second end of said capacitor element (C2) with the other of said source and said drain connected to said boost potential output terminal, and a third capacitor element (C_O) connected between said boost potential output terminal and a ref-

erence potential node, said boost voltage producing circuit (2A) characterized by further comprising:

a fourth capacitor element (C3) connected between the first end of said first capacitor element (C1) and the gate of said third transistor (Q3);

a fifth capacitor element (C4) connected between the first end of said second capacitor element (C2) and the gate of said fourth transistor (Q4);

a fifth transistor (Q5) having either a source or a drain connected to the second end of said first capacitor element (C1) with the other of said source and said drain connected to the gate of said third transistor (Q3) and a gate connected to the second end of said second capacitor element (C2); and

a sixth transistor (Q6) having either a source or a drain connected to the second end of said second capacitor element (C2) with the other of said source and said drain connected to the gate of said fourth transistor (Q4) and a gate connected to the second end of said first capacitor element (C1).

2. A boost voltage generating circuit according to claim 1, wherein said timing control circuit (2B,2C) is for generating, in addition to said first and second control signals (Φ1,Φ2), a third control signal (Φ3) which turns to a power supply potential level after said first control signal becomes a level of the power supply potential and turns to a level of said reference potential before said first control signal becomes the reference potential level, and a fourth control signal (Φ4) which turns to the power supply potential level after said second control signal becomes the power supply potential level and turns to the reference potential level before said second control signal becomes the reference potential level, and wherein a first end of said fourth capacitor element (C3) is separated from said first end of said first capacitor element (C1) and receives said third control signal (Φ3) and a first end of said fifth capacitor element (C4) is separated from said first end of said second capacitor element (C2) and receives said fourth control signal (Φ4).

3. A boost voltage generating circuit according to claim 2, further comprising a first level conversion circuit (3a) which converts the power supply potential level of said third control signal (Φ3) into a level-converted third control signal (Φ3a) with a level higher by a predetermined level and a second level conversion circuit (3b) which converts the power supply potential level of said fourth control signal (Φ4) into a level-converted fourth control signal (Φ4a) with a level higher by a predetermined level, said level-converted third control signal (Φ3a) being inputted to the first end of said fourth capacitor element (C3) and said level-converted fourth control signal (Φ4a) being inputted to the first end of said fifth capacitor element (C4).

4. A boost voltage generating circuit according to claim 1, wherein said first through sixth transistors (Φ1 through Q6) are N-channel field effect transistors.

5. A boost voltage generating circuit characterized by comprising:

a first, a second, a third and a fourth input terminal receiving a first (Φ1), a second (Φ2), a third (Φ3) and a fourth timing control signal (Φ4), respectively;

an output terminal (V_{OUT});

a first (N1), a second (N2), a third (N3) and a fourth circuit node (N4);

a power terminal (V_{CC});

a first transistor (Q1) having a gate connected with said second circuit node, and a source and a drain coupled between said power terminal and said first circuit node;

a second transistor (Q2) having a gate connected with said first circuit node, and a source and a drain coupled between said power terminal and said second circuit node;

a third transistor (Q3) having a gate connected with said third circuit node, and a source and a drain coupled between said first circuit node and said output terminal;

a fourth transistor (Q4) having a gate connected with said fourth circuit node, and a source and a drain coupled between said second circuit node and said output terminal;

a fifth transistor (Q5) having a gate connected with said second circuit node, and a source and a drain coupled between said first and said third circuit nodes;

a sixth transistor (Q6) having a gate connected with said first circuit node, and a source and a drain coupled between said second and said fourth circuit nodes;

a first capacitor (C1) coupled between said first input terminal and said first circuit node;

a second capacitor (C2) coupled between said second input terminal and said second circuit node;

a third capacitor (C3) coupled between said third input terminal and said third circuit node; and

a fourth capacitor (C4) coupled between

said fourth input terminal and said fourth circuit node.

6. A boost voltage generating circuit according to claim 5, wherein said first and said third input terminals are connected each other and said first and said third timing control signals (Φ1,Φ3) have the same waveform, and said second end said fourth input terminals are connected each other and said second and said fourth timing control signals (Φ2,Φ4) have the same waveform.

7. A boost voltage generating circuit according to claim 5, wherein said first and said third input terminals are separated and said first and said third timing control signals (Φ1,Φ3) have waveforms synchronized each other, and said second and said fourth input terminals are separated and said second and said fourth timing control signals (Φ2,Φ4) have waveforms synchronized each other.

8. A boost voltage generating circuit according to claim 7, wherein levels of said third and said fourth timing control signals (Φ3,Φ4) are boosted to levels higher than those of said first and said second timing control signals (Φ1,Φ2), respectively.

FIG. 1A
PRIOR ART

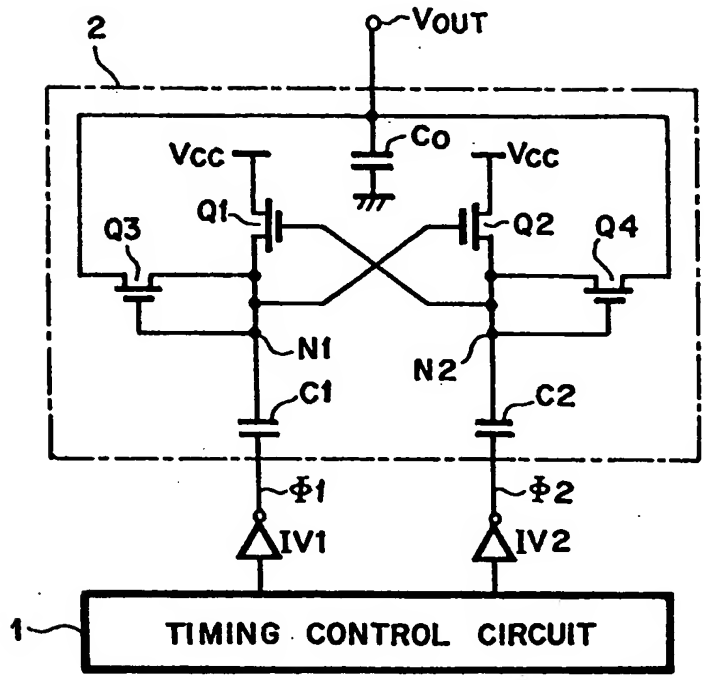


FIG. 1B
PRIOR ART

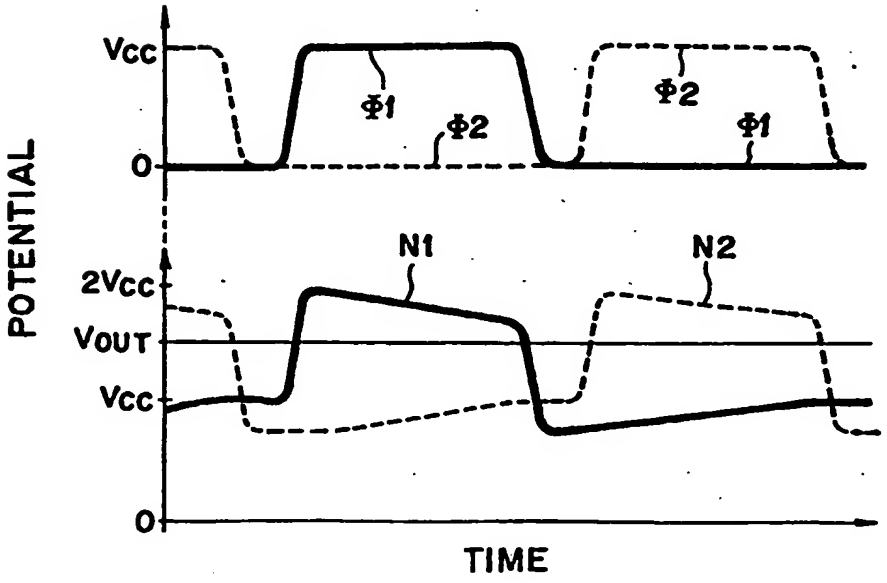


FIG. 2A

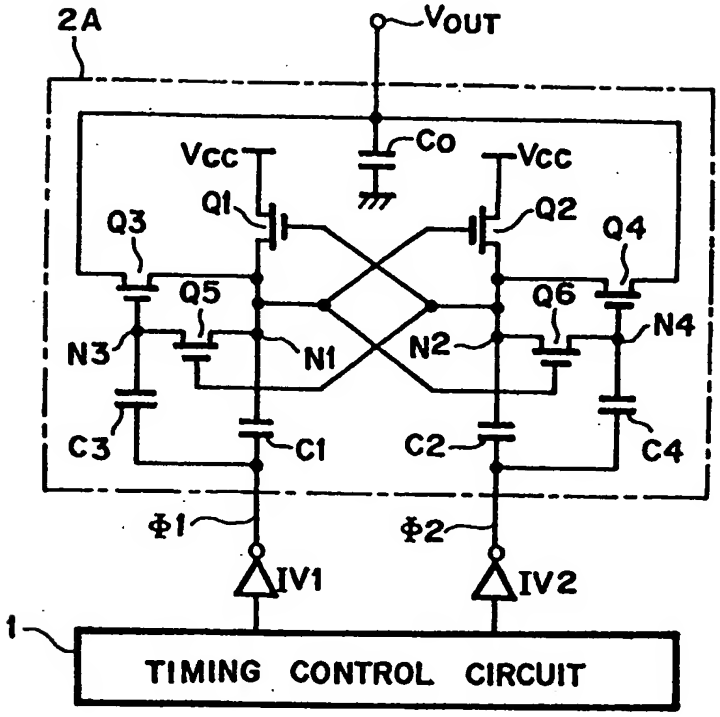

2A
VOUT
CO
Vcc
Vcc
Q1
Q2
Q3
Q4
Q5
Q6
N3
N1
N2
N4
C3
C1
C2
C4
Φ1
Φ2
IV1
IV2
1
TIMING CONTROL CIRCUIT

FIG. 2B

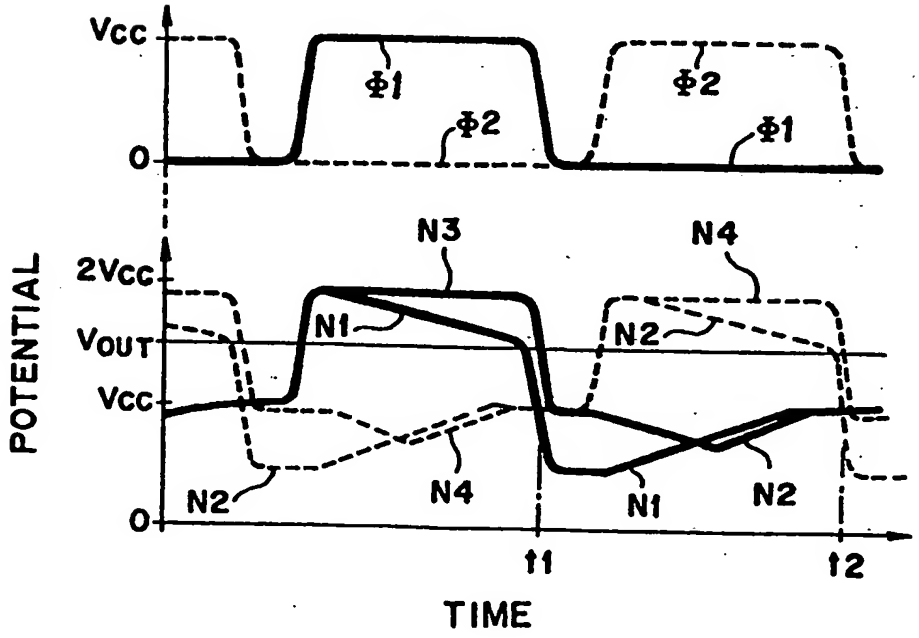

Vcc
0
Φ1
Φ2
Φ2
Φ1
POTENTIAL
2Vcc
VOUT
Vcc
0
N3
N4
N1
N2
N2
N4
N1
N2
t1
t2
TIME

FIG. 3A

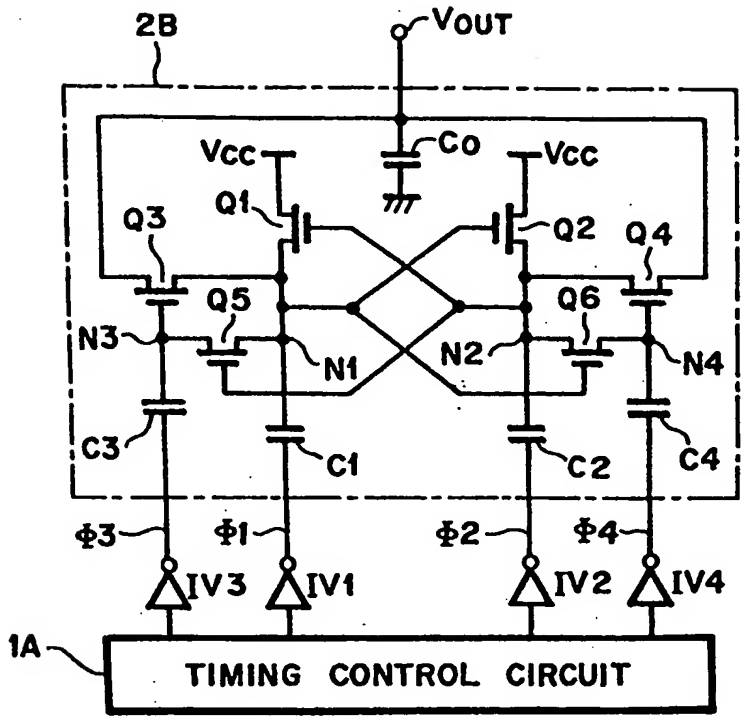

2B
VOUT
Vcc
Co
Vcc
Q1
Q3
Q2
Q4
Q5
Q6
N3
N1
N2
N4
C3
C1
C2
C4
Φ3
Φ1
Φ2
Φ4
IV3
IV1
IV2
IV4
1A
TIMING CONTROL CIRCUIT

FIG. 3B

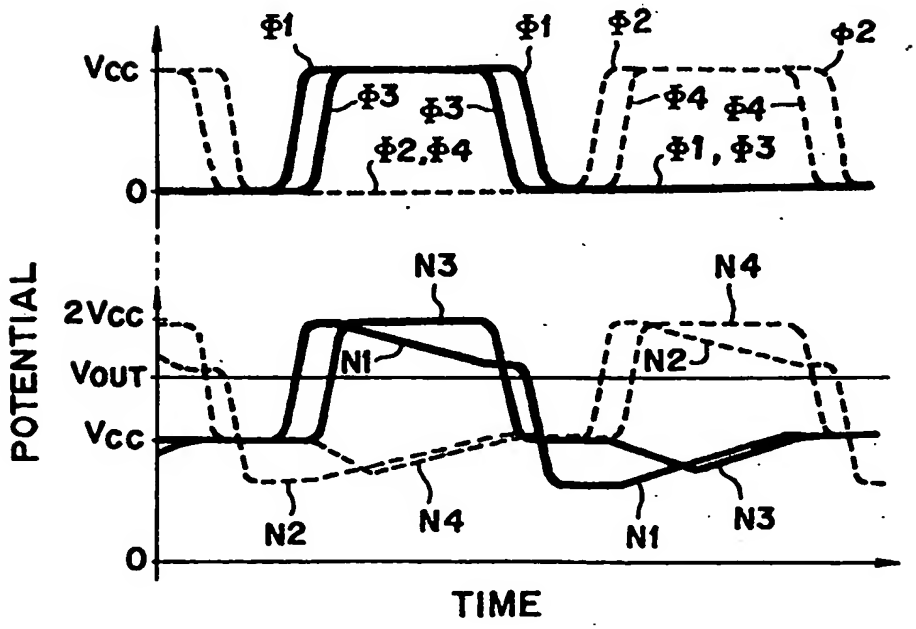

Φ1
Φ1
Φ2
Φ2
Vcc
Φ3
Φ3
Φ4
Φ4
Φ2,Φ4
Φ1, Φ3
0
N3
N4
POTENTIAL
2Vcc
N1
N2
VOUT
Vcc
N2
N4
N1
N3
0
TIME

FIG. 4A

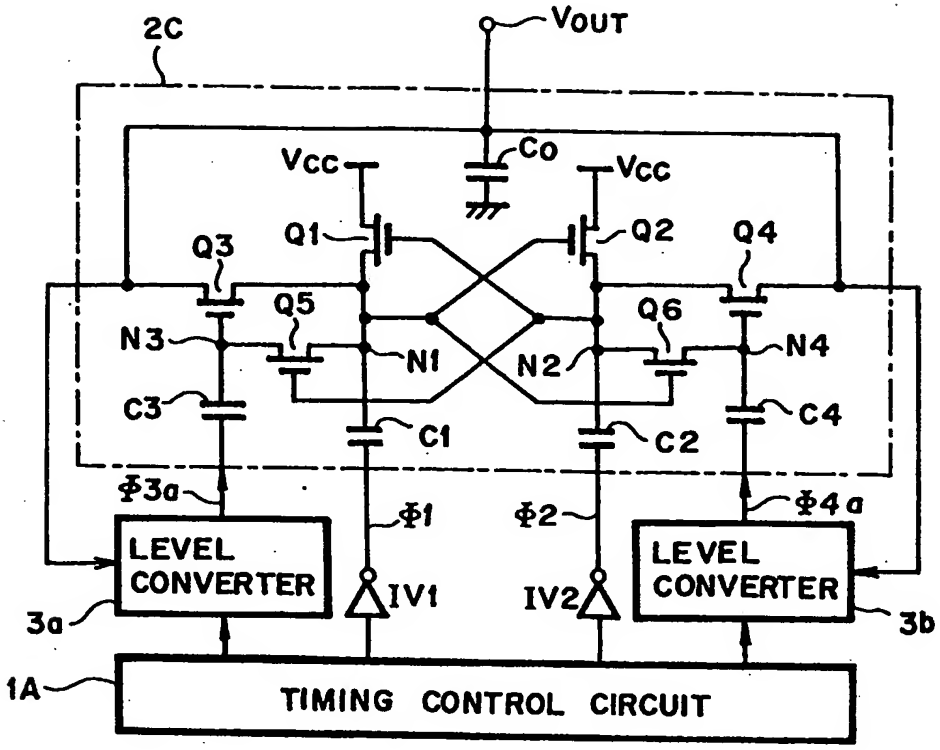
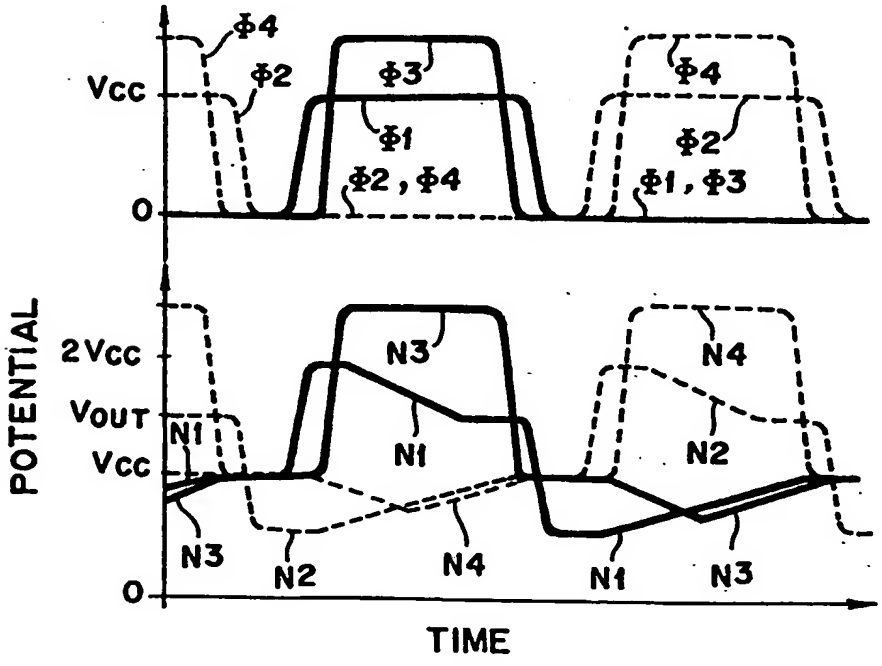

2C
VOUT
Vcc
Co
Vcc
Q3
Q1
Q2
Q4
Q5
Q6
N3
N1
N2
N4
C3
C1
C2
C4
Φ3a
Φ1
Φ2
Φ4a
LEVEL CONVERTER
IV1
IV2
LEVEL CONVERTER
3a
3b
1A
TIMING CONTROL CIRCUIT

FIG. 4B


Φ4
Φ2
Φ3
Φ1
Φ2, Φ4
Φ4
Φ2
Φ1, Φ3
Vcc
0
POTENTIAL
2Vcc
VOUT
Vcc
N1
N3
N1
N4
N2
N3
N2
N4
N1
N3
0
TIME